

R1EX24016ASAS0A

R1EX24016ATAS0A

Two-wire serial interface
16k EEPROM (2-kword × 8-bit)

REJ03C0350-0100

Rev.1.00

Apr. 21, 2008

Description

R1EX24xxx series are two-wire serial interface EEPROM (Electrically Erasable and Programmable ROM). They realize high speed, low power consumption and a high level of reliability by employing advanced MNOS memory technology and CMOS process and low voltage circuitry technology. They also have a 16-byte page programming function to make their write operation faster.

Note: Renesas Technology's serial EEPROM are authorized for using consumer applications such as cellular phone, camcorders, audio equipment. Therefore, please contact Renesas Technology's sales office before using industrial applications such as automotive systems, embedded controllers, and meters.

Features

- Single supply: 1.8 V to 5.5 V
- Two-wire serial interface (I²C serial bus)
- Clock frequency: 400 kHz
- Power dissipation:
 - Standby: 2 μA (max)
 - Active (Read): 1 mA (max)
 - Active (Write): 3.0 mA (max)
- Automatic page write: 16-byte/page
- Write cycle time: 5 ms
- Endurance: 10⁶ Cycles
- Data retention: 10 Years

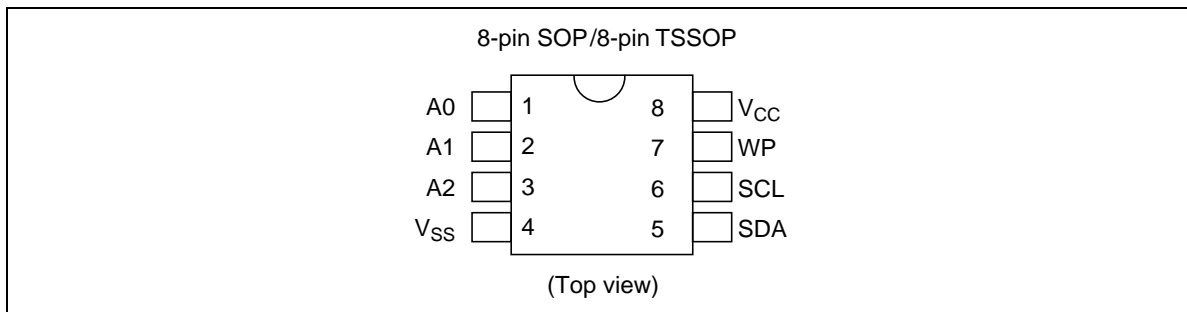
R1EX24016AxxS0A

- Small size packages: SOP-8pin, TSSOP-8pin
- Shipping tape and reel
 - TSSOP 8-pin: 3,000 IC/reel
 - SOP 8-pin: 2,500 IC/reel
- Temperature range: -40 to +85°C
- Lead free products.

Ordering Information

| Type No. | Internal organization | Operating voltage | Frequency | Package |
|-----------------|---------------------------|-------------------|-----------|---|
| R1EX24016ASAS0A | 16k bit (2048 × 8-bit) | 1.8 V to 5.5 V | 400 kHz | 150 mil 8-pin plastic SOP PRSP0008DF-B (FP-8DBV) Lead free |
| R1EX24016ATAS0A | 16k bit (2048 × 8-bit) | 1.8 V to 5.5 V | 400 kHz | 8-pin plastic TSSOP PTSP0008JC-B (TTP-8DAV) Lead free |

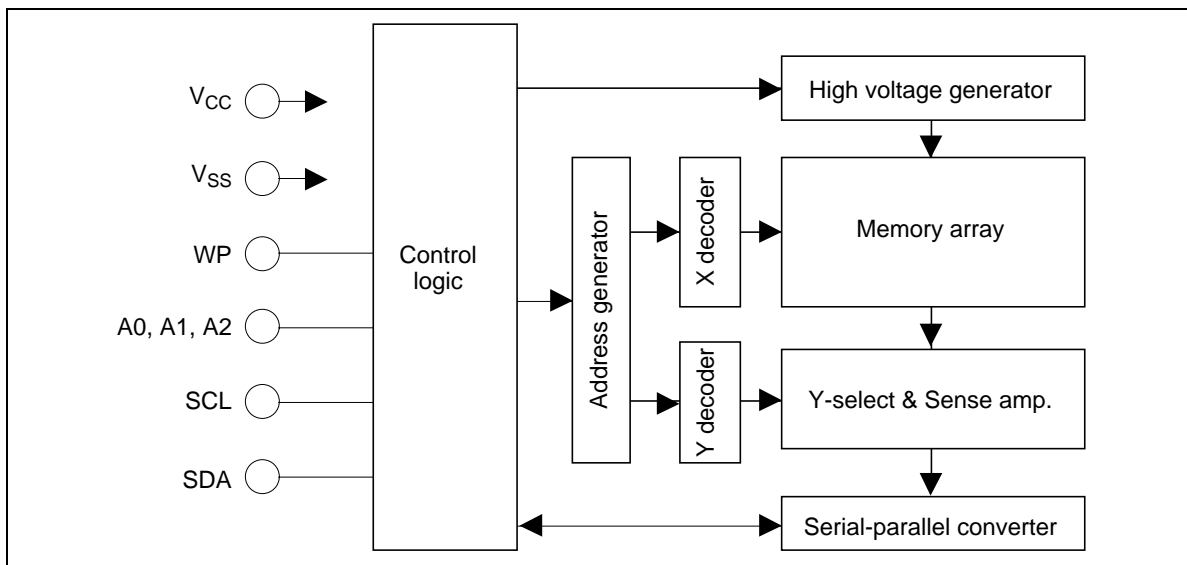
Pin Arrangement



Pin Description

| Pin name | Function |
|-----------------|--------------------------|
| A0 to A2 | Device address |
| SCL | Serial clock input |
| SDA | Serial data input/output |
| WP | Write protect |
| V _{CC} | Power supply |
| V _{SS} | Ground |
| NC | No connection |

Block Diagram



Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|--|-----------------|--|------|
| Supply voltage relative to V _{SS} | V _{CC} | -0.6 to +7.0 | V |
| Input voltage relative to V _{SS} | V _{in} | -0.5* ² to +7.0* ³ | V |
| Operating temperature range* ¹ | Topr | -40 to +85 | °C |
| Storage temperature range | Tstg | -55 to +125 | °C |

- Notes: 1. Including electrical characteristics and data retention.
 2. V_{in} (min): -3.0 V for pulse width ≤ 50 ns.
 3. Should not exceed V_{CC} + 1.0 V.

DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|-----------------------|----------|---------------------|-----|---------------------|------|
| Supply voltage | V_{CC} | 1.8 | — | 5.5 | V |
| | V_{SS} | 0 | 0 | 0 | V |
| Input high voltage | V_{IH} | $V_{CC} \times 0.7$ | — | $V_{CC} + 0.5$ | V |
| Input low voltage | V_{IL} | -0.3^{*1} | — | $V_{CC} \times 0.3$ | V |
| Operating temperature | Topr | -40 | — | +85 | °C |

Notes: 1. V_{IL} (min): -1.0 V for pulse width ≤ 50 ns.

DC Characteristics (Ta = -40 to +85°C, V_{CC} = 1.8 V to 5.5 V)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---------------------------------|-----------|-----|-----|-----|------|--|
| Input leakage current | I_{LI} | — | — | 2.0 | μA | $V_{CC} = 5.5$ V, $V_{in} = 0$ to 5.5 V |
| Output leakage current | I_{LO} | — | — | 2.0 | μA | $V_{CC} = 5.5$ V, $V_{out} = 0$ to 5.5 V |
| Standby V _{CC} current | I_{SB} | — | 1.0 | 2.0 | μA | $V_{in} = V_{SS}$ or V_{CC} |
| Read V _{CC} current | I_{CC1} | — | — | 1.0 | mA | $V_{CC} = 5.5$ V, Read at 400 kHz |
| Write V _{CC} current | I_{CC2} | — | — | 3.0 | mA | $V_{CC} = 5.5$ V, Write at 400 kHz |
| Output low voltage | V_{OL2} | — | — | 0.4 | V | $V_{CC} = 2.7$ to 5.5 V, $I_{OL} = 3.0$ mA |
| | V_{OL1} | — | — | 0.2 | V | $V_{CC} = 1.8$ to 2.7 V, $I_{OL} = 1.5$ mA |

Capacitance (Ta = +25°C, f = 1 MHz)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---------------------------------------|---------------|-----|-----|-----|------|-----------------|
| Input capacitance (A0 to A2, SCL, WP) | C_{in}^{*1} | — | — | 6.0 | pF | $V_{in} = 0$ V |
| Output capacitance (SDA) | C_{IO}^{*1} | — | — | 6.0 | pF | $V_{out} = 0$ V |

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 1.8$ to 5.5 V)**Test Conditions**

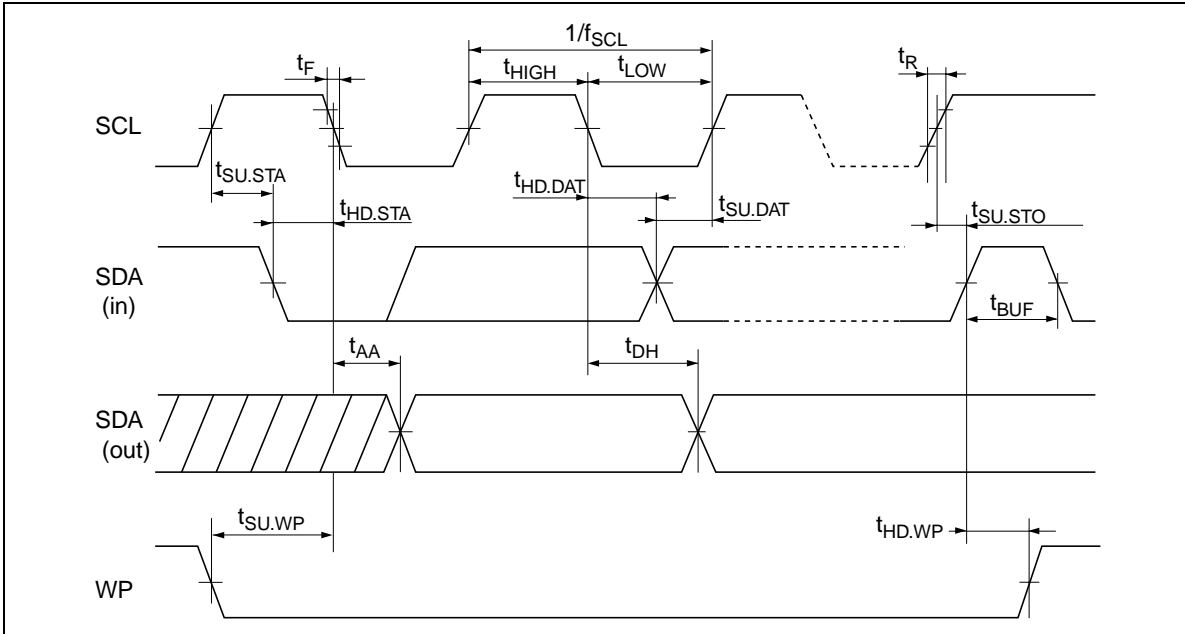
- Input pules levels:
 - $V_{IL} = 0.2 \times V_{CC}$
 - $V_{IH} = 0.8 \times V_{CC}$
- Input rise and fall time: ≤ 20 ns
- Input and output timing reference levels: $0.5 \times V_{CC}$
- Output load: TTL Gate + 100 pF

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|-----------------------------|--------------|------|--------|-----|--------|-------|
| Clock frequency | f_{SCL} | — | — | 400 | kHz | |
| Clock pulse width low | t_{LOW} | 1200 | — | — | ns | |
| Clock pulse width high | t_{HIGH} | 600 | — | — | ns | |
| Noise suppression time | t_I | — | — | 50 | ns | 1 |
| Access time | t_{AA} | 100 | — | 900 | ns | |
| Bus free time for next mode | t_{BUF} | 1200 | — | — | ns | |
| Start hold time | $t_{HD,STA}$ | 600 | — | — | ns | |
| Start setup time | $t_{SU,STA}$ | 600 | — | — | ns | |
| Data in hold time | $t_{HD,DAT}$ | 0 | — | — | ns | |
| Data in setup time | $t_{SU,DAT}$ | 100 | — | — | ns | |
| Input rise time | t_R | — | — | 300 | ns | 1 |
| Input fall time | t_F | — | — | 300 | ns | 1 |
| Stop setup time | $t_{SU,STO}$ | 600 | — | — | ns | |
| Data out hold time | t_{DH} | 50 | — | — | ns | |
| Write protect hold time | $t_{HD,WP}$ | 1200 | — | — | ns | |
| Write protect setup time | $t_{SU,WP}$ | 0 | — | — | ns | |
| Write cycle time | t_{WC} | — | — | 5 | ms | 2 |
| Erase/Write Endurance | — | — | 10^6 | — | cycles | 3 |

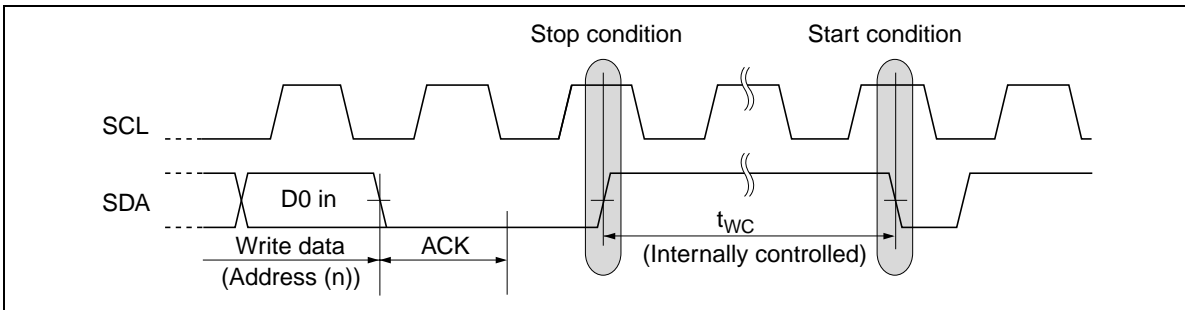
- Notes: 1. This parameter is sampled and not 100% tested.
2. t_{WC} is the time from a stop condition to the end of internally controlled write cycle.
3. This parameter is sampled and not 100% tested.
 10^6 Cycles ($T_a = 25^\circ\text{C}$)
 10^5 Cycles ($T_a = 85^\circ\text{C}$)

Timing Waveforms

Bus Timing



Write Cycle Timing



Pin Function

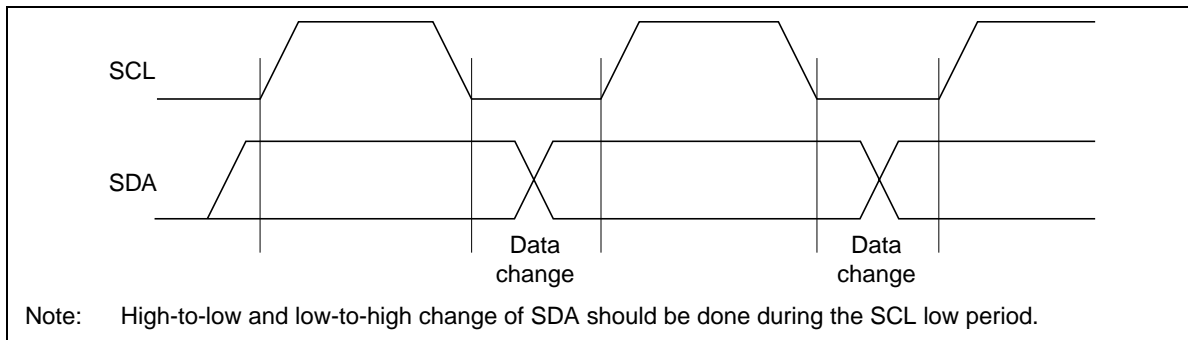
Serial Clock (SCL)

The SCL pin is used to control serial input/output data timing. The SCL input is used to positive edge clock data into EEPROM device and negative edge clock data out of each device. Maximum clock rate is 400 kHz.

Serial Input/Output Data (SDA)

The SDA pin is bidirectional for serial data transfer. The SDA pin needs to be pulled up by resistor as that pin is open-drain driven structure. Use proper resistor value for your system by considering V_{OL} , I_{OL} and the SDA pin capacitance. Except for a start condition and a stop condition which will be discussed later, the SDA transition needs to be completed during the SCL low period.

Data Validity (SDA data change timing waveform)



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Device Address (A0, A1, A2)

One device can be wired for one common data bus line as maximum. All device address are used for memory address, corresponding device address pins must not be fixed.

Pin Connections for A0 to A2

| Memory size | Max connect number | Pin connection | | | Note |
|-------------|--------------------|----------------|-----|-----|---|
| | | A2 | A1 | A0 | |
| 16k bit | 1 | x*1 | x*1 | x*1 | Use A0,A1,A2 for memory address a8,a9 and a10 |

Note: 1. Floating state can be possible.

Write Protect (WP)

When the Write Protect pin (WP) is high, the write protection feature is enabled and operates as shown in the following table.

Also, acknowledgment "0" is outputted after inputting device address and memory address. After inputting write data, acknowledgment "1" (**NO ACK**) is outputted.

When the WP is low, write operation for all memory arrays are allowed. The read operation is always activated irrespective of the WP pin status.

Write Protect Area

| WP pin status | Write protect area |
|---------------|-----------------------------|
| | 16k bit |
| V_{IH} | Full (16k bit) |
| V_{IL} | Normal read/write operation |

Functional Description

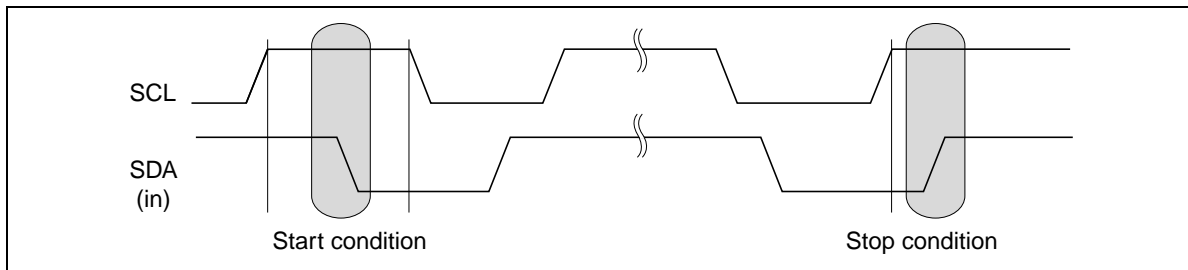
Start Condition

A high-to-low transition of the SDA with the SCL high is needed in order to start read, write operation (See start condition and stop condition).

Stop Condition

A low-to-high transition of the SDA with the SCL high is a stop condition. The stand-by operation starts after a read sequence by a stop condition. In the case of write operation, a stop condition terminates the write data inputs and place the device in a internally-timed write cycle to the memories. After the internally-timed write cycle which is specified as t_{wc} , the device enters a standby mode (See write cycle timing).

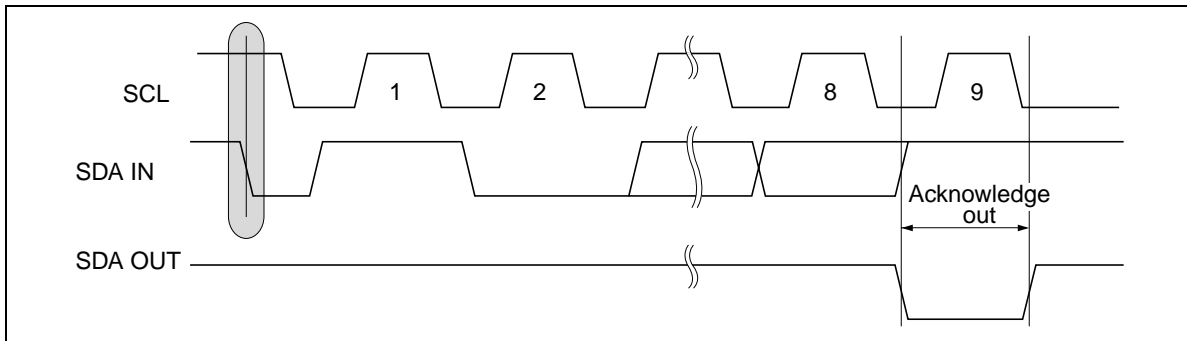
Start Condition and Stop Condition



Acknowledge

All addresses and data words are serially transmitted to and from in 8-bit words. The receiver sends a zero to acknowledge that it has received each word. This happens during ninth clock cycle. The transmitter keeps bus open to receive acknowledgment from the receiver at the ninth clock. In the write operation, EEPROM sends a zero to acknowledge after receiving every 8-bit words. In the read operation, EEPROM sends a zero to acknowledge after receiving the device address word. After sending read data, the EEPROM waits acknowledgment by keeping bus open. If the EEPROM receives zero as an acknowledge, it sends read data of next address. If the EEPROM receives acknowledgment "1" (no acknowledgment) and a following stop condition, it stops the read operation and enters a stand-by mode. If the EEPROM receives neither acknowledgment "0" nor a stop condition, the EEPROM keeps bus open without sending read data.

Acknowledge Timing Waveform



Device Addressing

The EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or a write operation. The device address word consists of 4-bit device code, 3-bit device address code and 1-bit read/write(R/W) code. The most significant 4-bit of the device address word are used to distinguish device type and this EEPROM uses “1010” fixed code. The device address code is followed by the 3-bit memory address in the order of a10, a9, a8.

The eighth bit of the device address word is the read/write(R/W) bit. A write operation is initiated if this bit is low and a read operation is initiated if this bit is high.

The EEPROM turns to a stand-by state if the device code is not “1010” or device address code doesn't coincide with status of the correspond hard-wired device address pins A0 to A2.

Device Address Word

| | Device address word (8-bit) | | | | | | | R/W code*1 |
|-----|-----------------------------|---|---|---|---------------------|----|----|------------|
| | Device code (fixed) | | | | Device address code | | | |
| 16k | 1 | 0 | 1 | 0 | a10 | a9 | a8 | R/W |

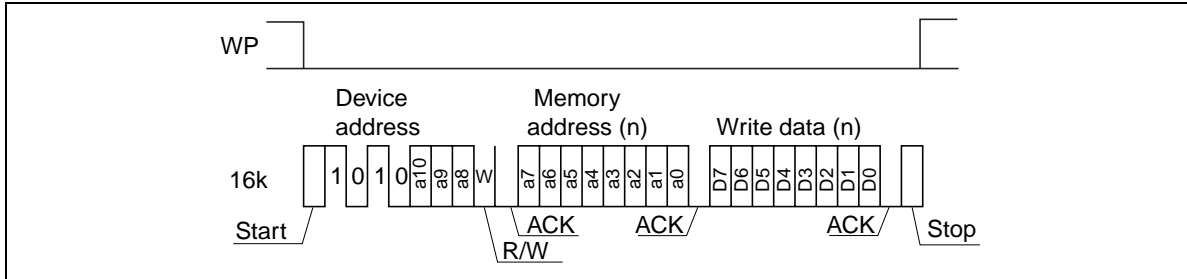
Note: 1. R/W=“1” is read and R/W = “0” is write.

Write Operations(WP=Low)

Byte Write: (Write operation during WP=Low status)

A write operation requires an 8-bit device address word with R/W = "0". Then the EEPROM sends acknowledgment "0" at the ninth clock cycle. After these, the 16kbit EEPROM receives 8-bit memory address words. Upon receipt of this memory address, the EEPROM outputs acknowledgment "0" and receives a following 8-bit write data. After receipt of write data, the EEPROM outputs acknowledgment "0". If the EEPROM receives a stop condition, the EEPROM enters an internally-timed write cycle and terminates receipt of SCL, SDA inputs until completion of the write cycle. The EEPROM returns to a standby mode after completion of the write cycle.

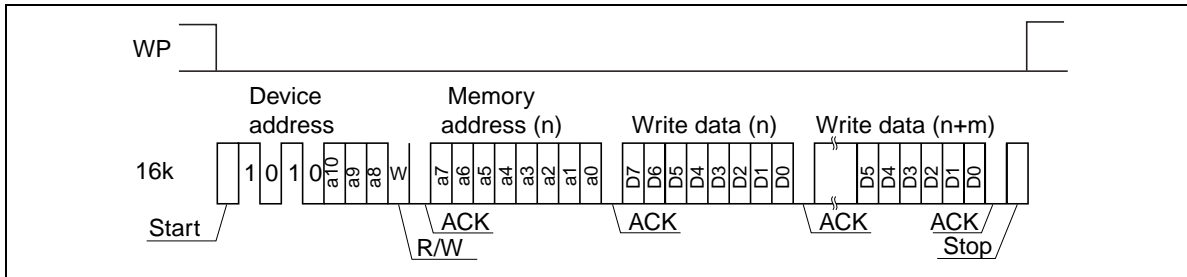
Byte Write Operation



Page Write:

The EEPROM is capable of the page write operation which allows any number of bytes up to 16 bytes to be written in a single write cycle. The page write is the same sequence as the byte write except for inputting the more write data. The page write is initiated by a start condition, device address word, memory address(n) and write data (Dn) with every ninth bit acknowledgment. The EEPROM enters the page write operation if the EEPROM receives more write data (Dn+1) instead of receiving a stop condition. The a0 to a3 address bits are automatically incremented upon receiving write data (Dn+1). The EEPROM can continue to receive write data up to 16 bytes. If the a0 to a3 address bits reaches the last address of the page, the a0 to a3 address bits will roll over to the first address of the same page and previous write data will be overwritten. Upon receiving a stop condition, the EEPROM stops receiving write data and enters internally-timed write cycle.

Page Write Operation



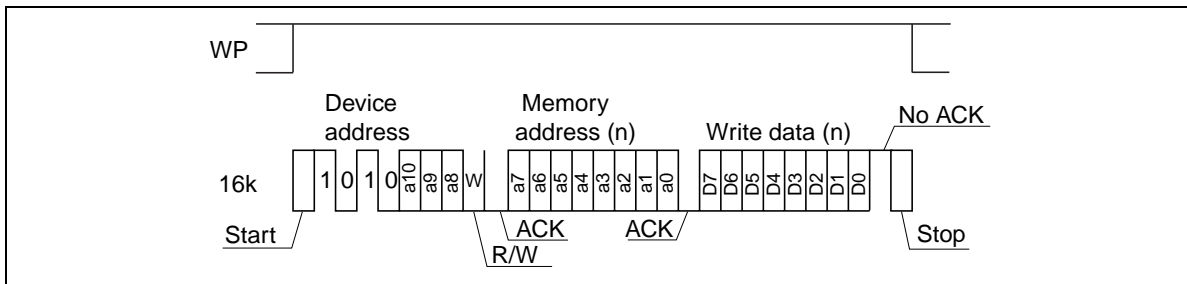
Write Operations(WP=High)

Byte Write: (Write operation during WP=High status)

A write operation requires an 8-bit device address word with R/W = "0". Then the EEPROM sends acknowledgment "0" at the ninth clock cycle. After these, the 16kbit EEPROM receives 8-bit memory address words.

Upon receipt of this memory address, the EEPROM outputs acknowledgment "0". After receipt of 8-bit write data, the EEPROM outputs acknowledgment "1"(NO ACK). Then the EEPROM write operations are not allowed.

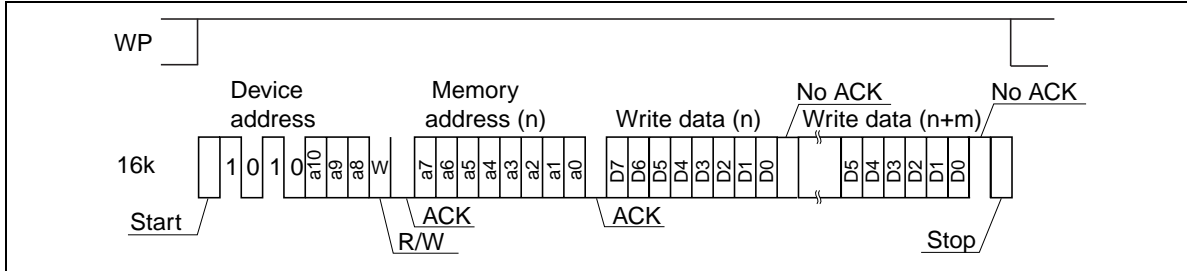
Byte Write Operation



Page Write:

The page write is the same sequence as the byte write. The page write is initiated by a start condition, device address word and memory address(n) with every ninth bit acknowledgment "0". But after inputting write data(Dn) , the EEPROM outputs acknowledgment "1"(NO ACK). Then the EEPROM write operations are not allowed.

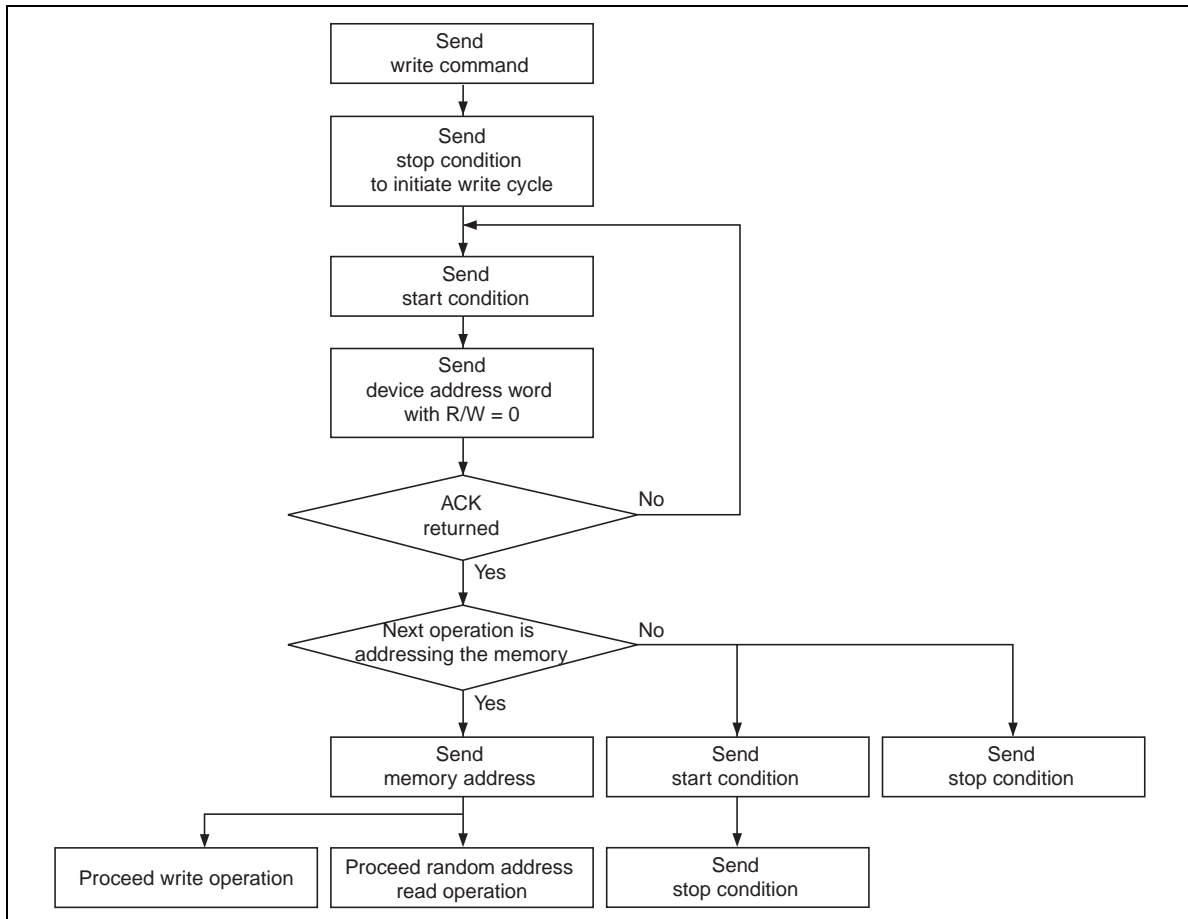
Page Write Operation



Acknowledge Polling:

Acknowledge polling feature is used to show if the EEPROM is in a internally-timed write cycle or not. This feature is initiated by the stop condition after inputting write data. This requires the 8-bit device address word following the start condition during a internally-timed write cycle. Acknowledge polling will operate when the R/W code = "0". Acknowledgment "1" (no acknowledgment) shows the EEPROM is in a internally-timed write cycle and acknowledgment "0" shows that the internally-timed write cycle has completed. See Write Cycle Polling using ACK.

Write Cycle Polling Using ACK



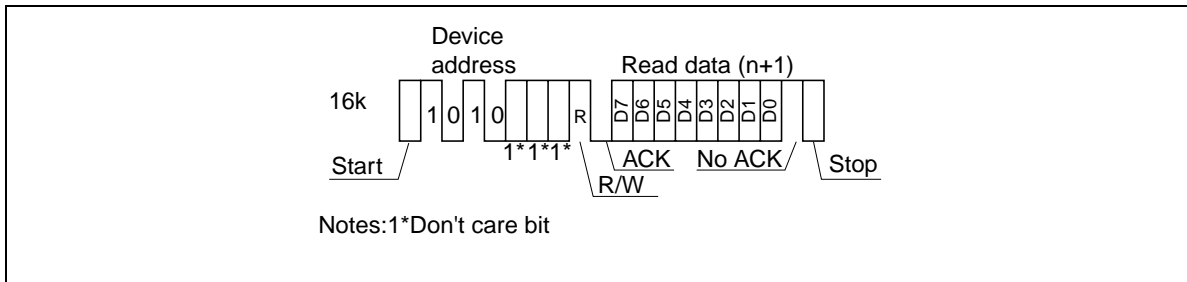
Read Operation

There are three read operations: current address read, random read, and sequential read. Read operations are initiated the same way as write operations with the exception of R/W = "1".

Current Address Read:

The internal address counter maintains the last address accessed during the last read or write operation, with incremented by one. Current address read accesses the address kept by the internal address counter. After receiving a start condition and the device address word (R/W is "1"), the EEPROM outputs the 8-bit current address data from the most significant bit following acknowledgment "0". If the EEPROM receives acknowledgment "1" (no acknowledgment) and a following stop condition, the EEPROM stops the read operation and is turned to a standby state. In case the EEPROM has accessed the last address of the last page at previous read operation, the current address will roll over and returns to zero address. In case the EEPROM has accessed the last address of the page at previous write operation, the current address will roll over within page addressing and returns to the first address in the same page. The current address is valid while power is on. The current address after power on will be indefinite. The random read operation described below is necessary to define the memory address.

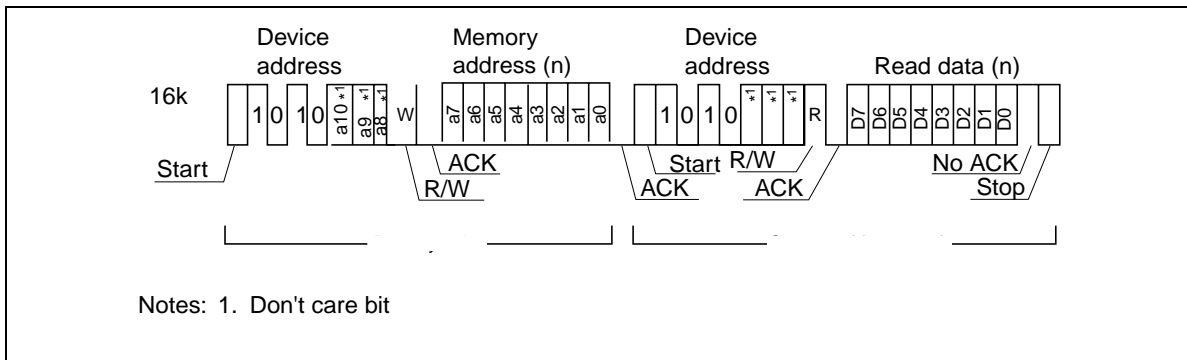
Current Address Read Operation



Random Read:

This is a read operation with defined read address. A random read requires a dummy write to set read address. The EEPROM receives a start condition, device address word (R/W=0) and memory address 2×8 -bit sequentially. The EEPROM outputs acknowledgment “0” after receiving memory address then enters a current address read with receiving a start condition. The EEPROM outputs the read data of the address which was defined in the dummy write operation. After receiving acknowledgment “1”(no acknowledgment) and a following stop condition, the EEPROM stops the random read operation and returns to a standby state.

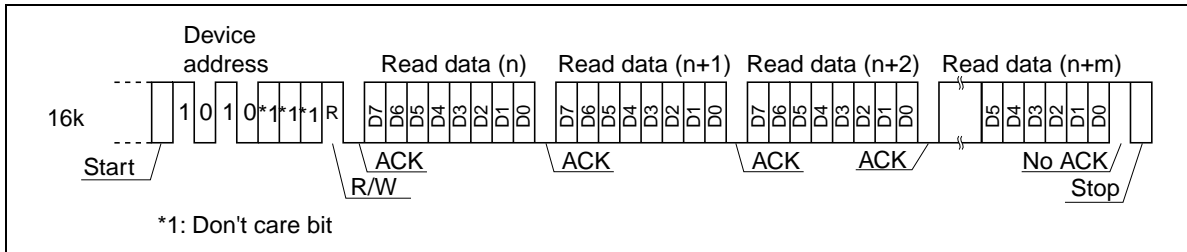
Random Read Operation



Sequential Read:

Sequential reads are initiated by either a current address read or a random read. If the EEPROM receives acknowledgment “0” after 8-bit read data, the read address is incremented and the next 8-bit read data are coming out. This operation can be continued as long as the EEPROM receives acknowledgment “0”. The address will roll over and returns address zero if it reaches the last address of the last page. The sequential read can be continued after roll over. The sequential read is terminated if the EEPROM receives acknowledgment “1” (no acknowledgment) and a following stop condition.

Sequential Read Operation



Notes

Data Protection at V_{cc} On/Off

When V_{cc} is turned on or off, noise on the SCL and SDA inputs generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to unintentional program mode. To prevent this unintentional programming, this EEPROM has a power on reset function. Be careful of the notices described below in order for the power on reset function to operate correctly.

- SCL and SDA should be fixed to V_{cc} or V_{ss} during V_{cc} on/off. Low to high or high to low transition during V_{cc} on/off may cause the trigger for the unintentional programming.
- V_{cc} should be turned off after the EEPROM is placed in a standby state.
- V_{cc} should be turned on from the ground level(V_{ss}) in order for the EEPROM not to enter the unintentional programming mode.
- V_{cc} turn on speed should be longer than 10 μ s.

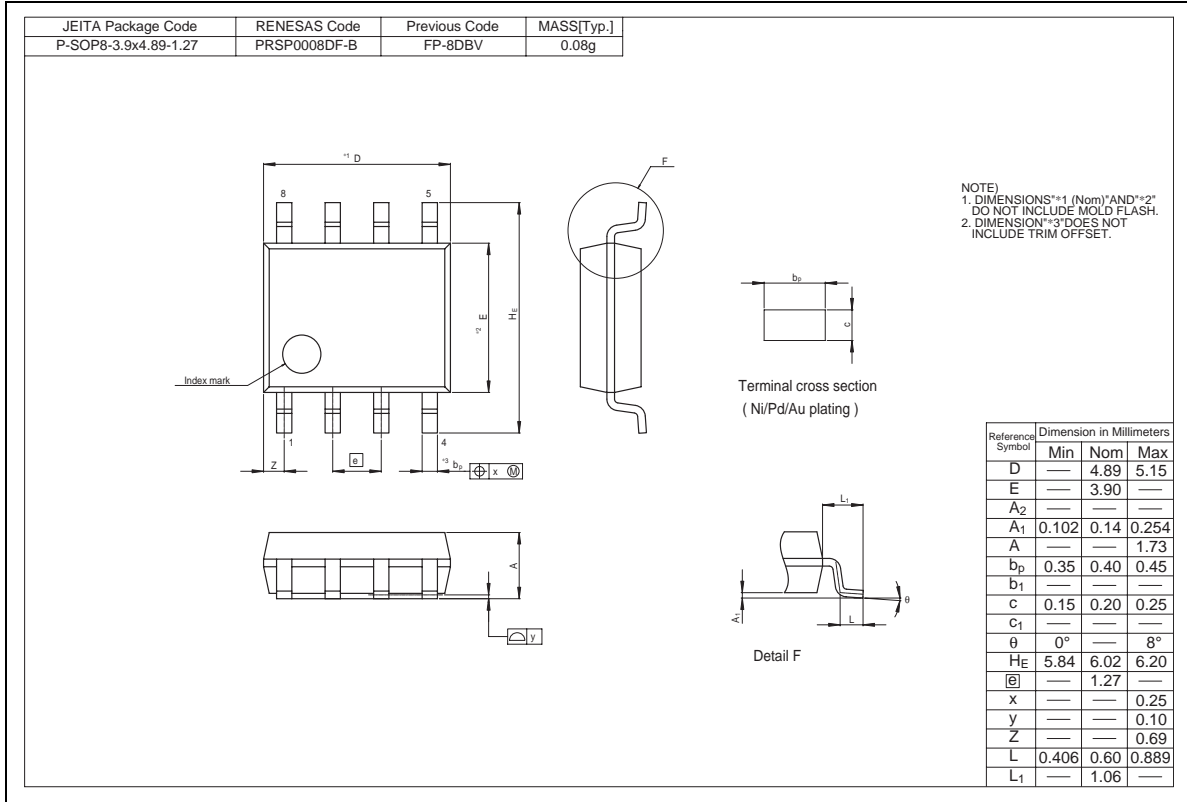
Noise Suppression Time

This EEPROM have a noise suppression function at SCL and SDA inputs, that cut noise of width less than 50 ns. Be careful not to allow noise of width more than 50 ns.

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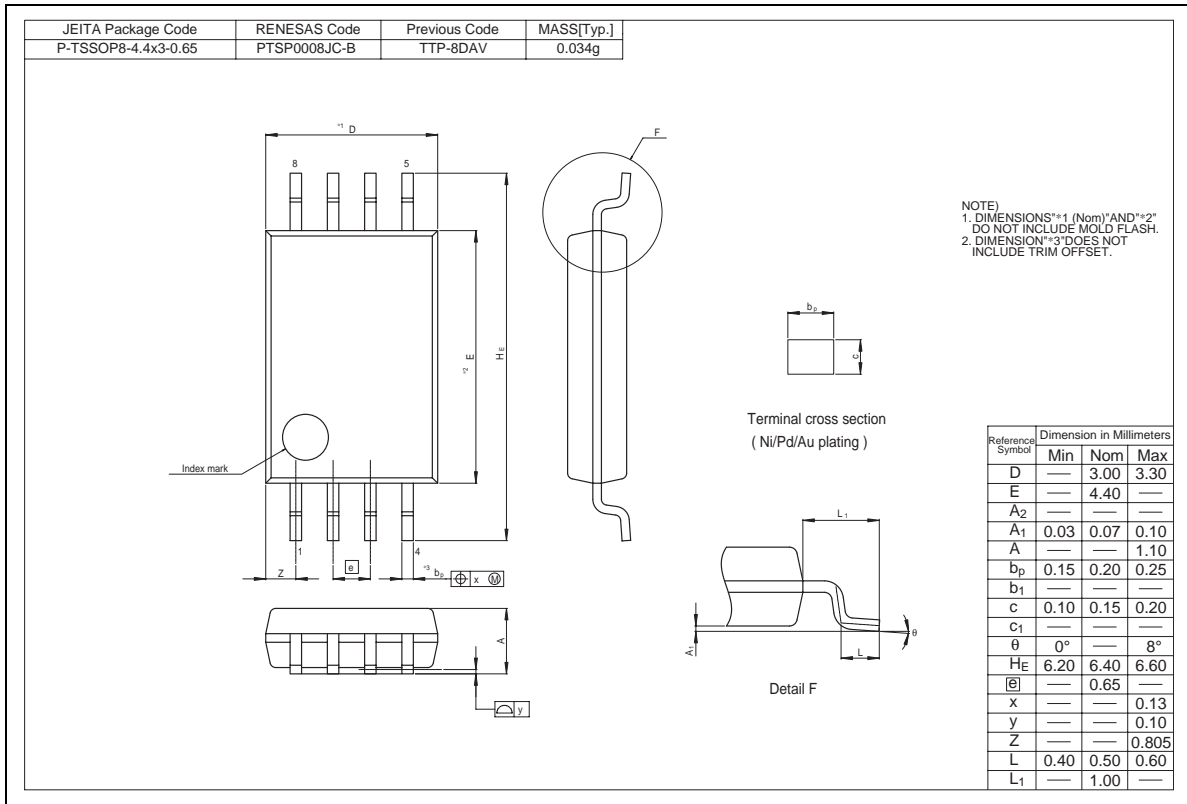
Package Dimensions

R1EX24016ASAS0A (PRSP0008DF-B / Previous Code: FP-8DBV)



R1EX24016AxxS0A

R1EX24016ATAS0A (PTSP0008JC-B / Previous Code: TTP-8DAV)



Revision History**R1EX24016AxxS0A Data Sheet**

| Rev. | Date | Contents of Modification | |
|------|-----------------|--------------------------|-------------------------|
| | | Page | Description |
| 0.01 | Dec. 26, 2007 | — | Initial issue |
| 1.00 | April. 21, 2008 | — | Deletion of preliminary |

Notes:

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